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An engineering approach to high-performance scannable flip-flops embedding functional logics

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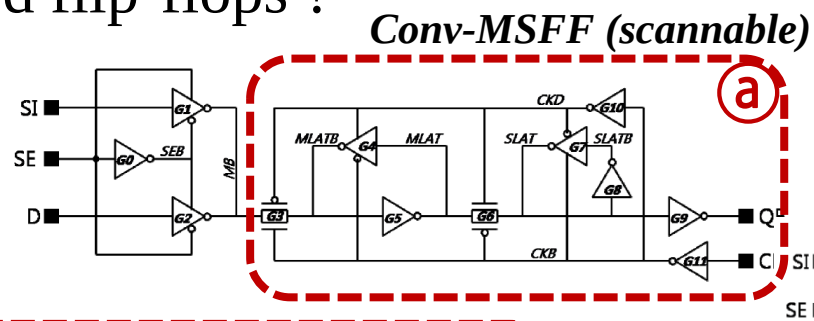
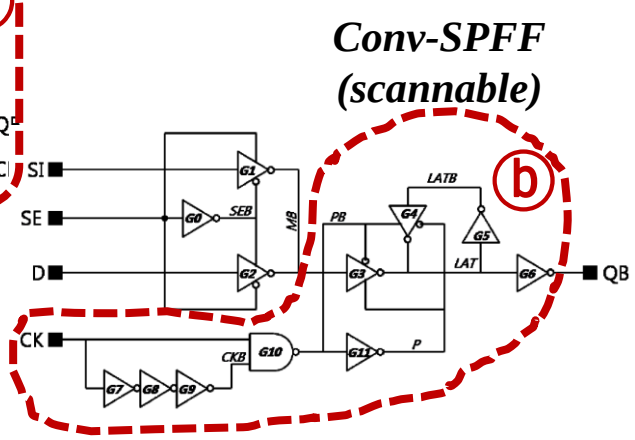
How have high-performance flip-flops conventionally been designed ?

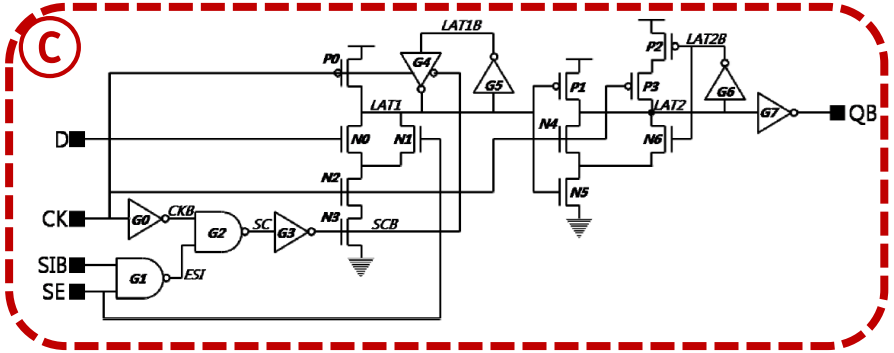
- Representative examples of high-speed flip-flops ?
  - ⓐ Master-slave flip-flops [1,2,5]
  - ⓑ Static-pulse flip-flops [5,6]
  - ⓒ Semi-dynamic flip-flops [4,5,7]

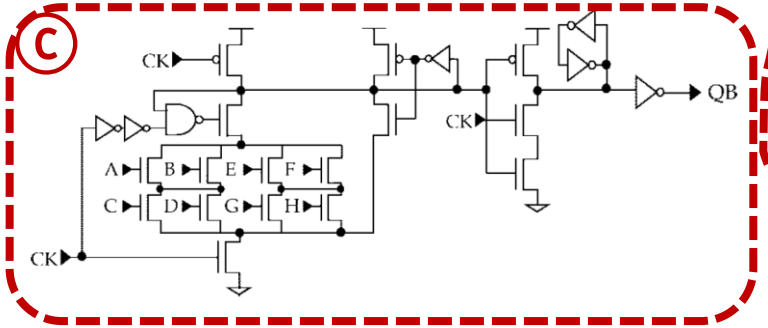
- Scannable
  - ⓓ LSSD scan [1,6]
  - ⓔ Mux scan [2,4]
  - ⓕ Scan-controlled [7]

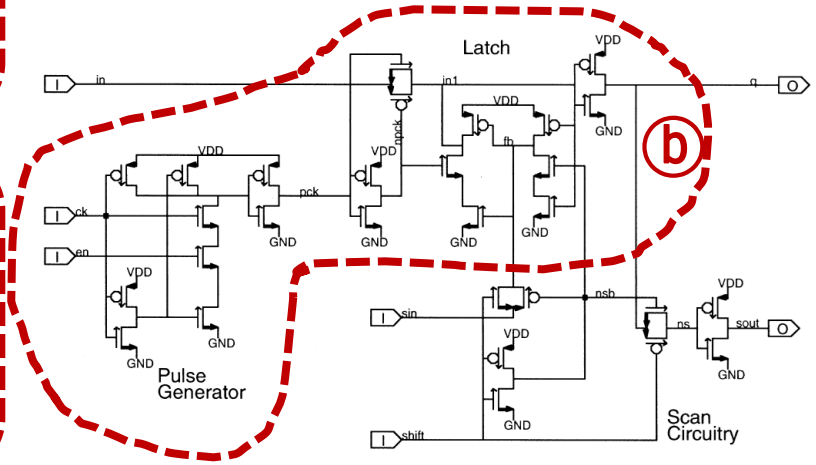
- Logic embedded
  - ⓖ CMOS logic [2]
  - ⓗ Dynamic logic [4,6]
  - ⓘ Clocked domino logic [3]











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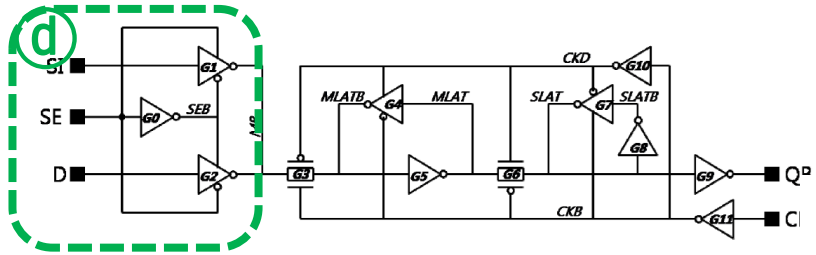

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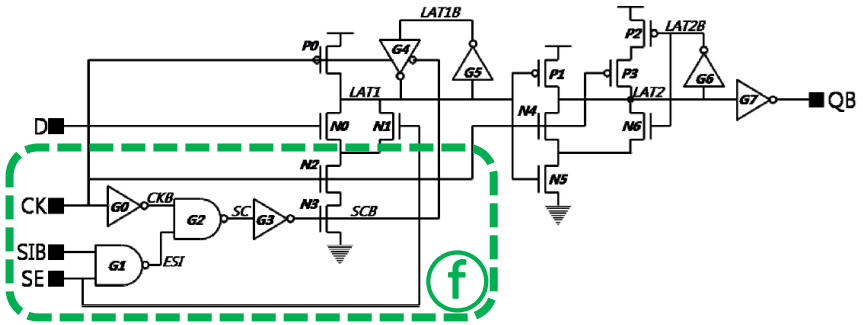

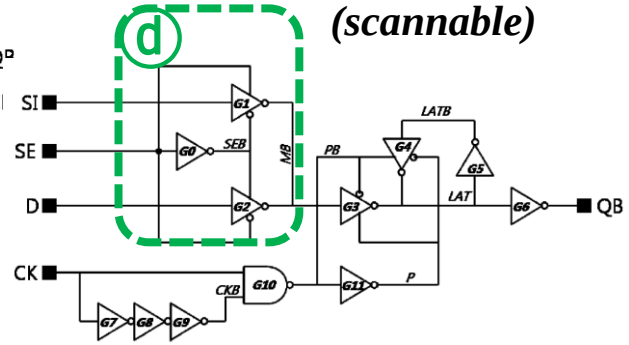

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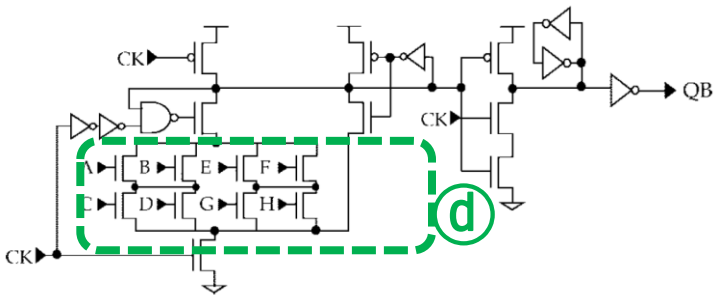

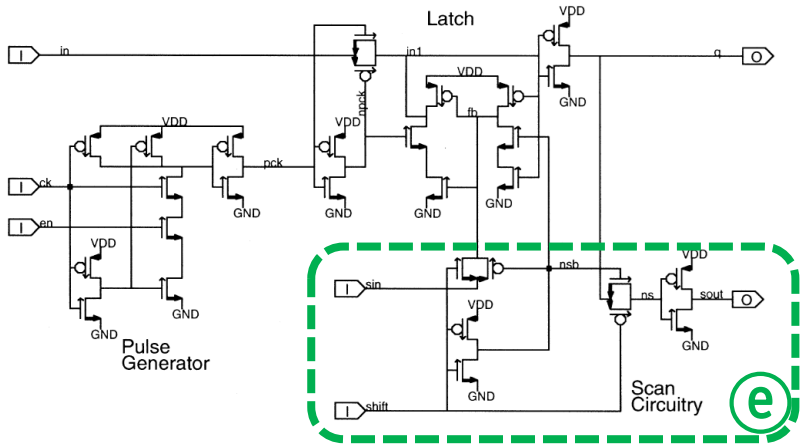

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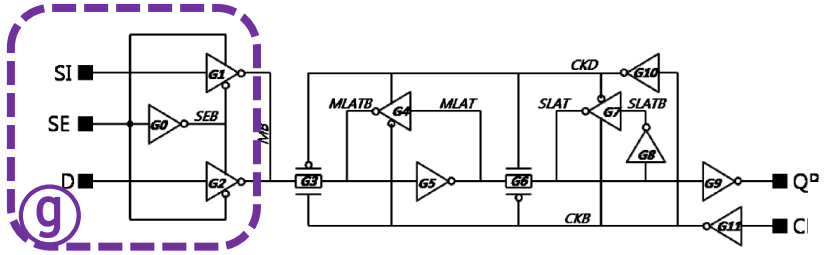
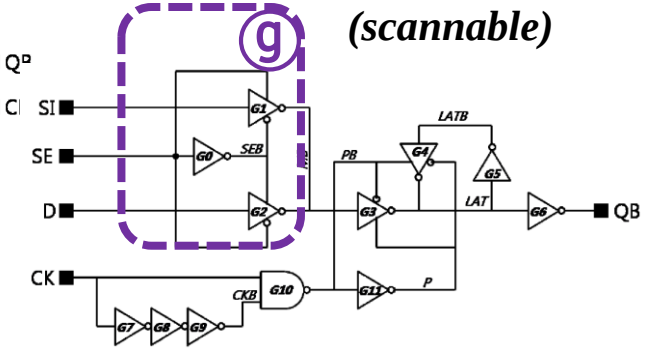


Conv-SPFF (scannable)



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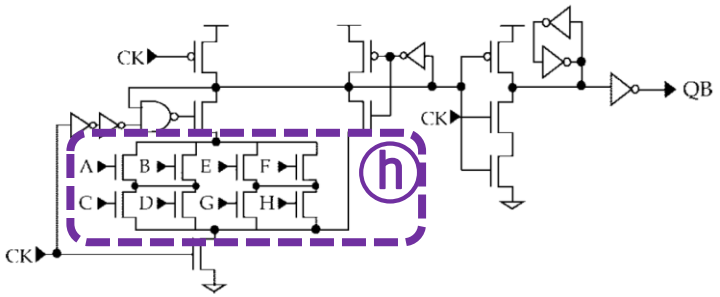

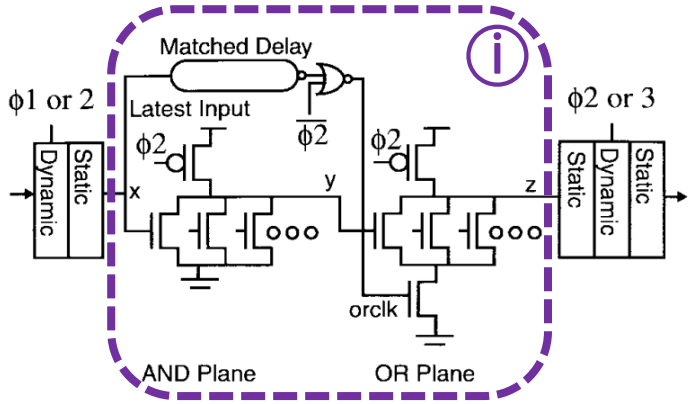

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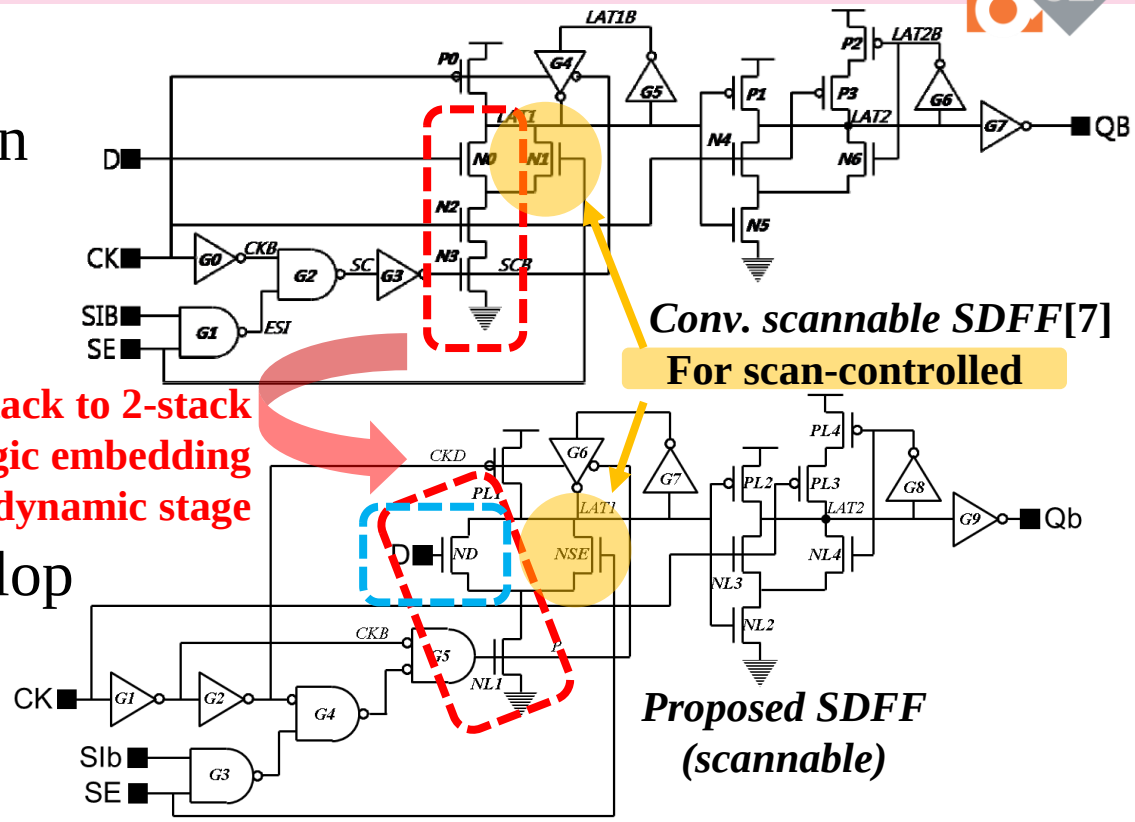
We have chosen the semi-dynamic flip-flop for logic-embedding

- Structural advantages
  - ✓ Faster evaluation of a complex logic function like a wide-OR gate
  - ✓ Less timing and power overheads for a scan implementation [7]

- Further optimization for logic-embedding
  - ✓ We propose a scannable semidynamic flip-flop having two-stack NMOS in dynamic stage.



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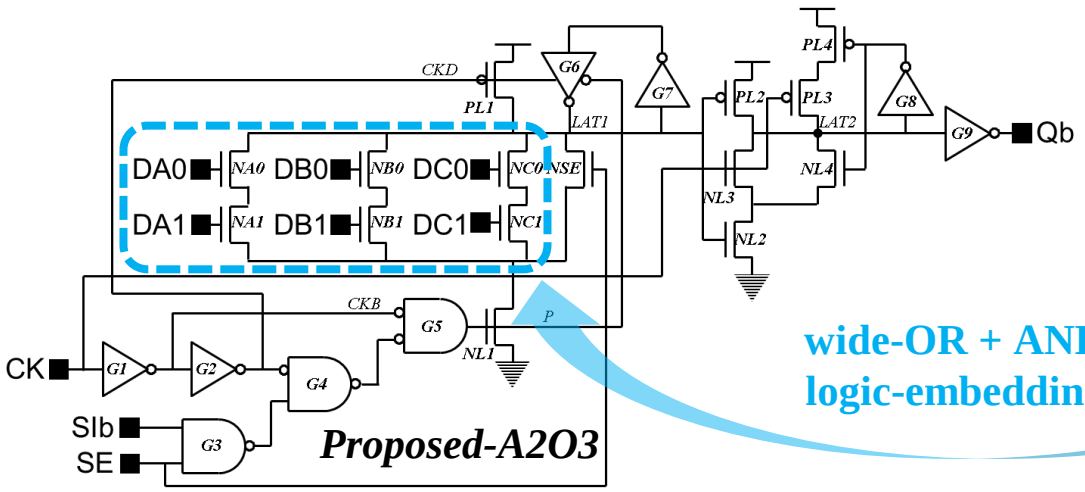
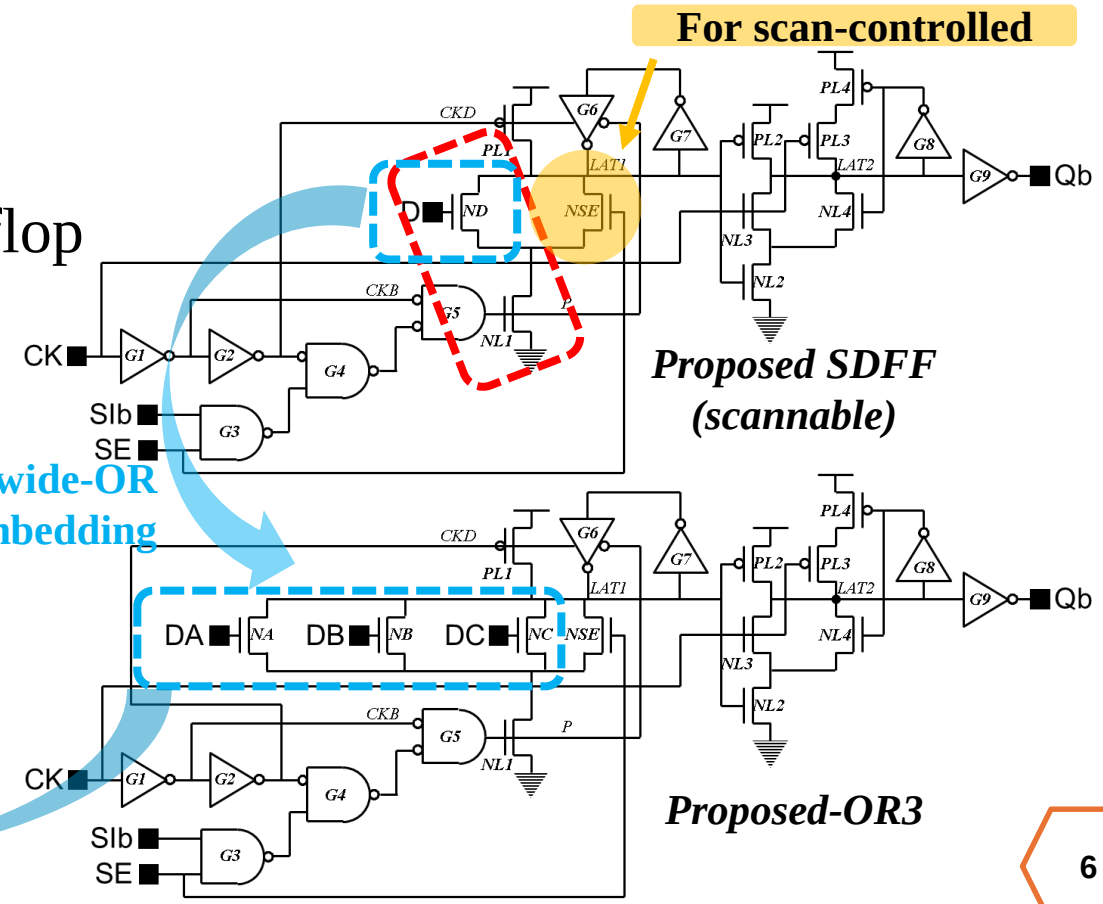


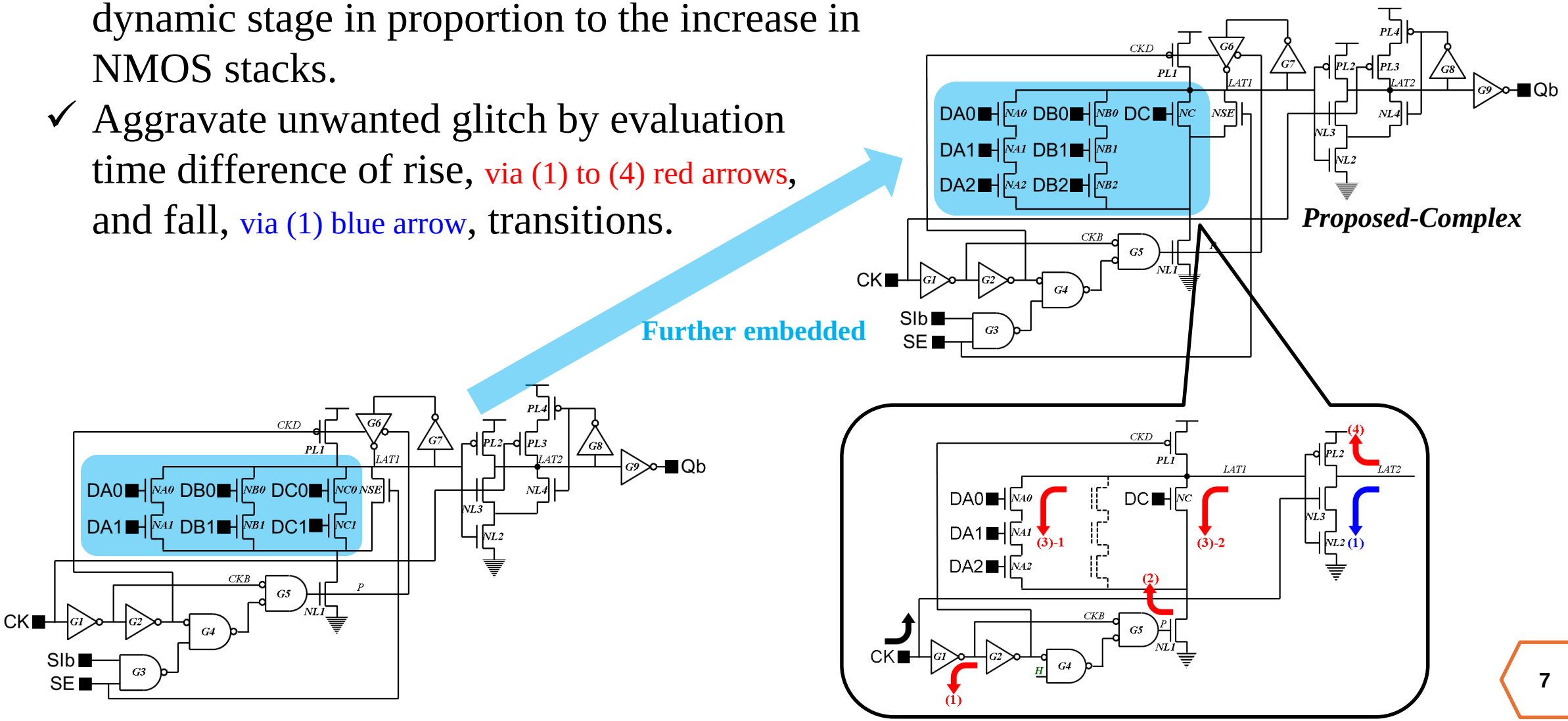
wide-OR + AND logic-embedding

wide-OR logic-embedding



Clocked domino logic has been adapted for further enhancement

- AND-logic, unlike wide-OR logic, leads to a large NMOS stack in the dynamic stage
  - ✓ Considerably degrades evaluation speed of the dynamic stage in proportion to the increase in NMOS stacks.
  - ✓ Aggravate unwanted glitch by evaluation time difference of rise, via (1) to (4) red arrows, and fall, via (1) blue arrow, transitions.



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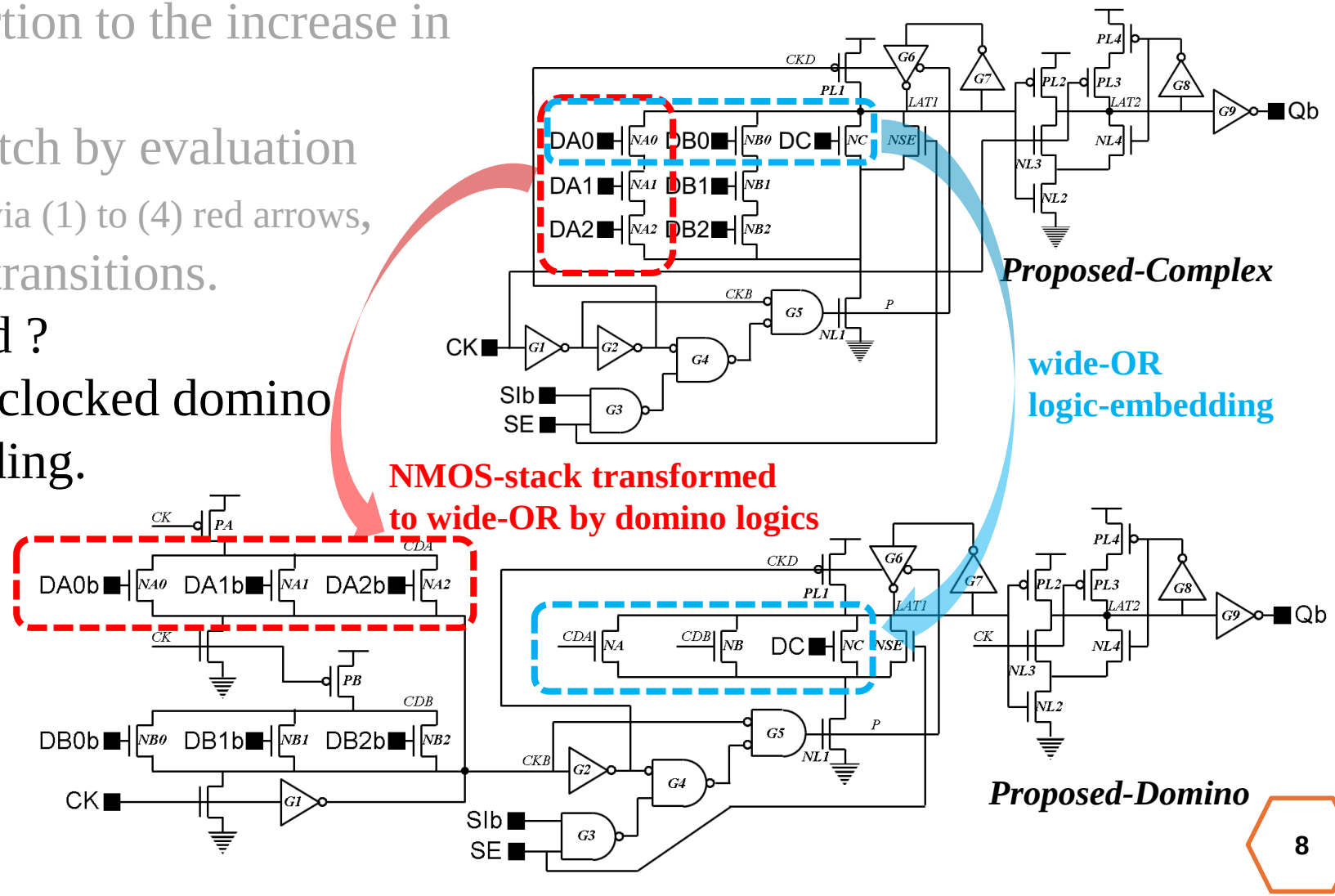
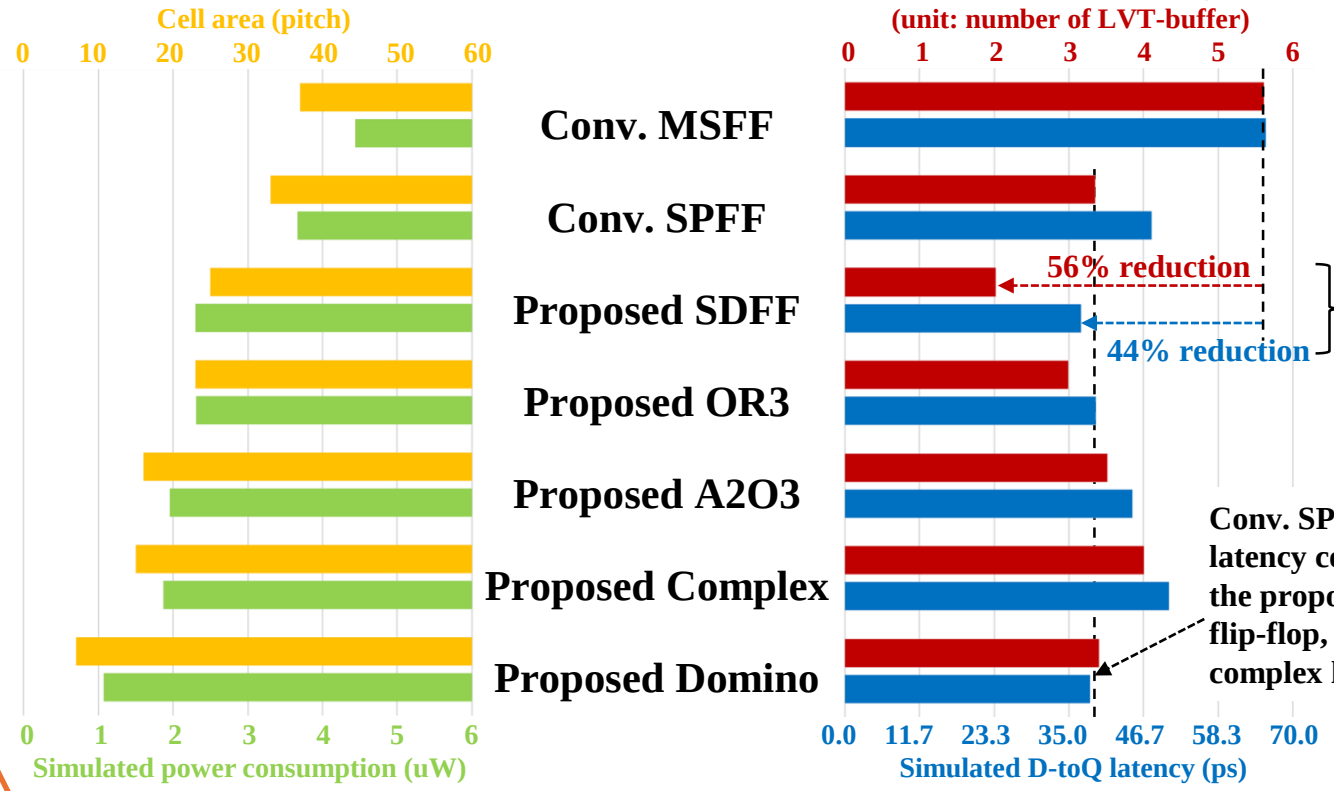
  - ✓ Aggravate unwanted glitch by evaluation time difference of rise, via (1) to (4) red arrows, and fall, via (1) blue arrow, transitions.
- How can this issue be solved ?
  - ✓ We propose a modified clocked domino for further logic embedding.

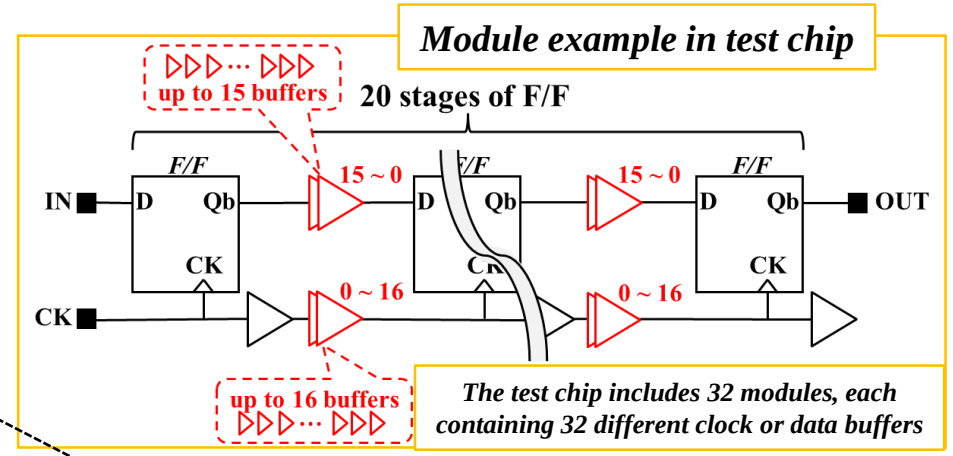


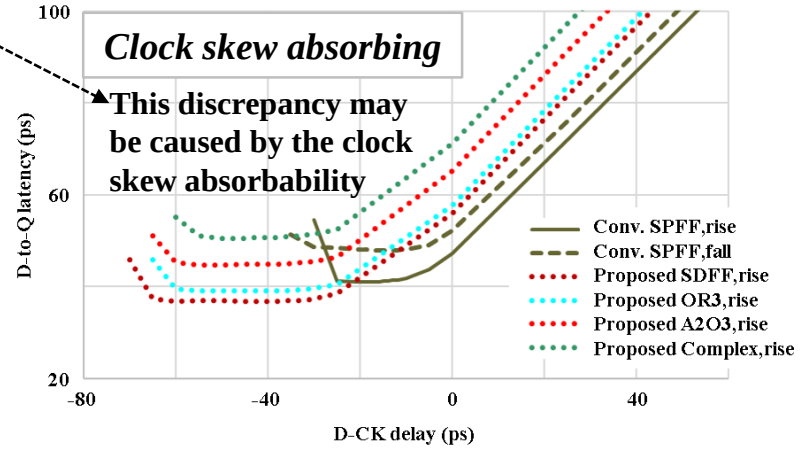
Simulated & Measured performance comparison

- The conventional and proposed flip-flops were physically designed to be compatible with a standard cell architecture, utilizing a 14nm FinFET process for both simulation and silicon fabrication. The flip-flops were optimized under the Slow-Slow (SS) corner for PMOS-NMOS with a regular threshold voltage (RVT) at 1.0V and 125°C.



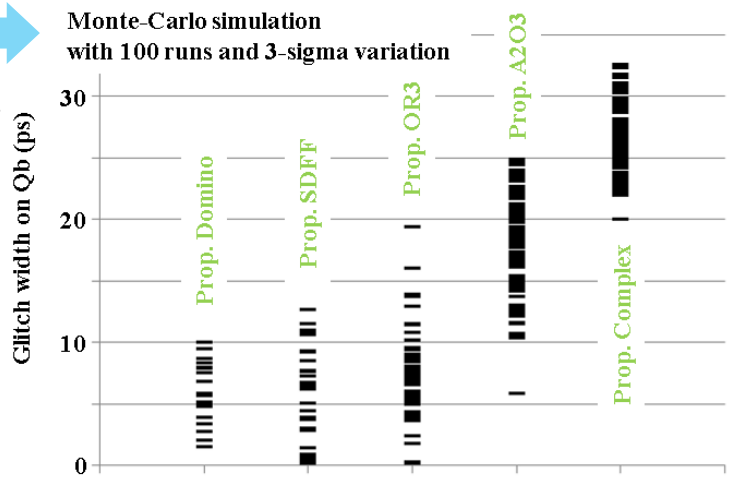
Conv. SPFF exhibits a D-to-Q latency comparable to that of the proposed logic-embedded flip-flop, even with the complex logic embedded

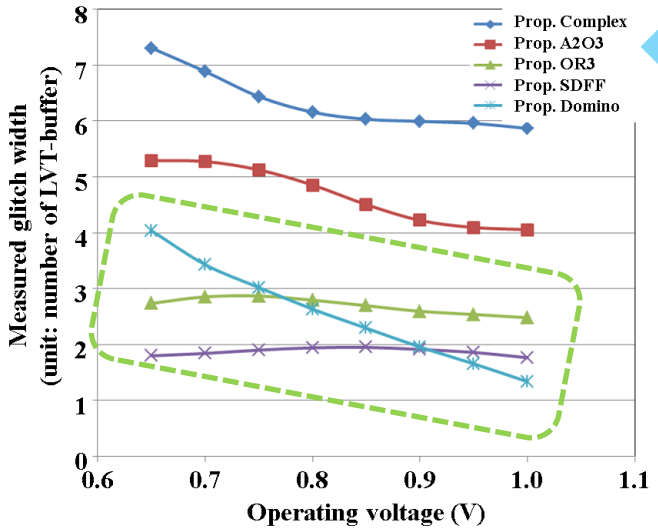


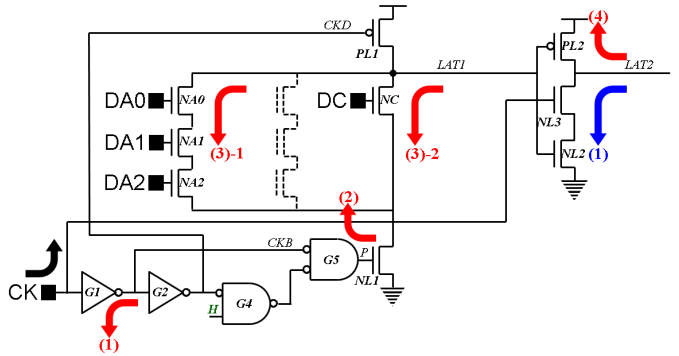


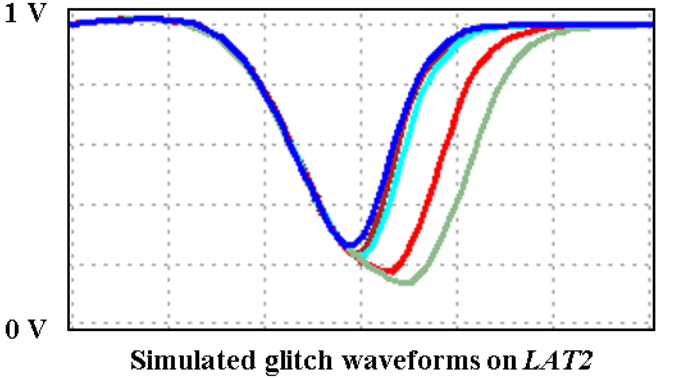
Output glitch comparison and summary

- The waveforms display output glitches on LAT2 and Qb nodes at the rise transition of CK when consecutive inputs are high.
  - ✓ At 1.00V, both simulation and measurement results indicate that Proposed Domino exhibits the smallest output glitch.
  - ✓ Until 0.65V, the output glitches of Proposed SDFF, Proposed OR3 and Proposed Domino remain still smaller.

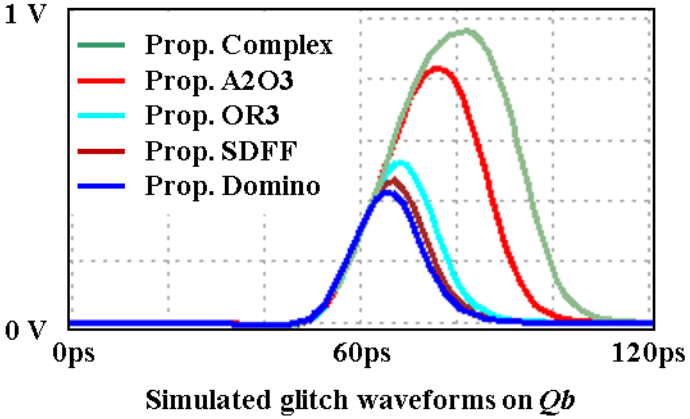








Simulated glitch waveforms on *LAT2*



Simulated glitch waveforms on *Qb*

Summary

- This approach addressed the key challenges of the slow evaluation time and the output glitches in the logic-embedded semi-dynamic flip-flops.
- To mitigate the slow evaluation caused by the embedded logics, the proposed scannable two-stack semi-dynamic flip-flop reduces NMOS stacking in the dynamic stage, enhancing speed.
- The proposed scannable logic-embedded flip-flop, with its modified clock-delayed domino structure, also improves performance, especially with the complex logic circuits.
- The silicon measurements on the 14nm FinFET process demonstrated the 56% improvement in D-to-Q latency for the proposed scannable two-stack flip-flop compared to the conventional master-slave design with the scan MUX.
- Furthermore, the proposed scannable logic-embedded flip-flop achieves D-to-Q latency close to that of the conventional static pulse-based flip-flop, even with the complex logic embedded.
- Additionally, the modification in the clock-delayed domino structure alleviates the output glitches, with the measured glitch width being 3 to 5 times smaller.